Can IP solutions trigger AS5643-2.0?

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1 Background

Back around the turn of the century a remarkable decision was made within the aerospace industry: following a comprehensive needs assessment, technology analysis and trade study Lockheed Martin (LMCO) decided to use IEEE1394b as the new avionics data bus for the world's largest and most strategic fighter jet program, i.e. the F-35 Lightening II. The decision came as a surprise to many technologists around the world, but for those who admired IEEE1394 it was the opportune time to see the technology blossom. Remember, that around this time IEEE1394 was losing popularity as a consumer electronics bus and it had started to disappear from cameras, laptops, computer, storage devices, etc., being replaced by other technologies such as HDMI, GigE & USB.

The selection by LMCO was all the more surprising as IEEE1394 was originally designed to address the requirements of a modern consumer electronics interconnect. It offers features and functions that in many areas go way beyond the needs of a typical Aerospace and Defense (A&D) interconnect technology, yet in other areas falls short of essential requirements of this specific market segment. For its use on the F-35 LMCO decided to use a subset of the IEEE1394 functionality and add extensions to make it "A&D usable", which included mechanisms for boosting reliability such as deterministic bus timing, anonymous subscriber messaging, fault tolerance and redundancy. Eventually, these efforts and the push to foster COTS development resulted in a new SAE standard, namely AS5643. Today, AS5643 is a standardized framework and is used in growing numbers in A&D programs all around the world.

With respect to the availability of components required for a suitable IEEE1394/AS5643 interface Texas Instruments (TI) became and nowadays is the sole source for IEEE1394 bus interface chips / chip sets. Unfortunately, the downturn in the consumer electronics market affected the supply/demand dynamics and, even within TI, the momentum driving IEEE1394 faded dramatically. Components used in A&D were transitioned to their HiREL product line, added mil-grade temperature stability and some minor bug fixes. However, with slowing demand, longer-than-expected RDT&E on F-35, etc., volume sales of IEEE1394 silicon remained low and TI could not afford an internal infrastructure to drive product innovation. Eventually this led to minimal support for the existing silicon. As of today the silicon used within A&D is old, buggy and no longer actively supported. So far, there has been no end-of-life (EOL) announcement for standard 1394 PHY and Link layer devices.

According to TI sources, there is a current effort to re-spin the critical network interconnectivity component (i.e. the PHY layer chip). Should this be implemented, it will be well received by the A&D community. Allegedly funded by US Government the new version should eliminate device bugs that have severely affected several ongoing A&D programs. However, this effort may not be addressing strategic enhancements towards built-in support for AS5643 within the silicon. As with any other off-the-shelf silicon available in the market at the moment this new PHY revision will likely only support the IEEE1394 level and may not be targeted at incorporating any of the AS5643 extensions.

In the big picture the A&D industry continues to view AS5643 as a novelty. The SAE Standard has a few, yet powerful early adopters but even though the adoption of AS5643 is growing, dependence on a single IEEE1394 silicon source without a product roadmap leaves many technology decision makers uneasy. Interestingly, the perceived "uncertainty" has also opened the door for new and innovative approaches. Today's IP based solutions are on the verge of taking over the IEEE1394 interface market and are on the doorstep of replacing the usage of IEEE1394 silicon. FPGAs have become extremely powerful as well as versatile and the additional HW cost can by far be offset with benefits like feature extensions, reprogrammability, upgradability, etc. Especially for SOC-designs combing processing functionality together with multiple instances of the I/O interface in one single HW component appeal not only to design engineers but also to individuals concerned about sustainability, supportability, compatibility and longevity.

2 Is AS5643-2.0 really needed?

Technologically, AS5643 can go far beyond its current form and iteration. It needs to be pointed out that the existing SAE standard was based on what was technically possible at the time when the F-35 system architecture was defined.

LMCO's intension at the onset was to use off-the-shelf I/O silicon in order to bring down costs and, given the large quantities of consumer electronics with IEEE1394, they seemed to be on the right path for cost reduction and continued innovation. However, as mentioned earlier the consumer market for 1394 faded and this left the A&D industry with a very small supplier base for sourcing usable IEEE1394 silicon.

In some way AS5643-1.0 has been a testing & proving ground and has demonstrated successfully its benefits and readiness in the F-35 program. These 5th generation fighter jets have matured beyond their initial development phase and are now on the verge for full rate production and deployment. From an adoption-of-the-technology point of view, F-35 is a done deal.

So what does this mean for AS5643 as an emerging avionics interface and interconnectivity solution? It's future will depend on maintaining or improving the adoption rate of the technology. Several large aerospace programs are on the horizon in the US, in Europe as well as in Asia with USA-based examples being the NGAD - 6th generation fighter and MQ-25 Stingray unmanned tanker. Yet, some critical questions still exist for AS5643. What will ensure the adoption of AS5643 by these programs? What will help sell AS5643 as a viable technology in the future? What will fuel the momentum and growth that has been created for AS5643?

- Is it the fact that the current version of AS5643 is in the air with the F-35? Is it the slowly yet steadily growing number of components and solutions? Has AS5643 really reached a "critical mass" and are the components really "COTS"?

- Or is it that like other technologies AS5643 has a technology roadmap? Will a new program decide to use AS5643 because of its technological advances and benefits?

- Or will it be a combination, i.e. a mix of technological advances together with a cost reduction?

Since IEEE1394 was regarded as a new bus technology for aircraft flight control, designing & developing a control system based on IEEE1394 for the F-35 likely was a formidable and costly undertaking for LMCO. Yet, now that the development is more or less completed, any attempts to apply similar costs as comparison for future programs would be unfair. Prices will certainly come down as more and more COTS products become available. But legacy solutions (1553, etc.) will continue to present some challenge: they are deeply integrated into several systems within multiple programs, have reached a high level of maturity and have become cost effective. AS5643 will continue to fight for its market share with said technologies. Therefore, moving forward it will be key to continue with the technological evolution with emphasis on expanding the AS5643 features and functions.

3 IP offers a jump-start to AS5643 innovation

The possibilities of using IP for A&D have one key aspect: innovative ideas can be implemented, tested and matured for usage in an A&D-suitable and approved HW platform yet still provide the flexibility very much like SW. In-field upgradability and the ability of system debugging in case things go wrong are features that cannot be provided by off-the-shelf silicon in general. It should be noted that once a specific technological feature becomes "mainstream" the silicon industry can consider integrating it within an existing design which can then be re-spun in silicon. But the market potential and technical demands need to be proven and verified and IP offers just the right approach for this!

Within the SAE AS1-3 Working Group, discussions had started how a standardized set of optimized AS5643 functions can be defined to ensure multi-vendor device interoperability. As a multi-vendor environment continues to be important (for the purpose of cost reduction and business risk mitigation) the need of test bed compatibility and compliance verification arises. Yet, the entire effort is governed by the premise of maintaining compliance with the current revision of the AS5643 standard, compatibility with current programs and leverage of investments made by system and/or LRU vendors based on revision of the standard. The author of this paper understands the technological needs of current programs as well as business investments already made by various parties. The "backward compatibility" approach mentioned above has its merits. Yet, the author of this paper suggests a much further-going approach which has only become possible with the availability, maturity and the growing willingness to deploy such solutions by the A&D industry. We believe that the time has come to work on the standardization of a "true" AS5643

solution. AS5643-2.0 could be a stand-alone avionics network connectivity standard and not just an add-on to IEEE1394.

The true benefits of IP solutions cannot be described more eloquently than by analyzing the options towards an implementation for a few examples of much needed functional enhancement:

a) Connection Status Monitoring. Standard IEEE1394 silicon offers only minimal functionality regarding monitoring of the device-device connectivity stability. The only built-in feature is a readable register that counts transmission errors. In a real world scenario with degrading quality of the interconnect (cable, transceivers, ….) this is hardly enough information. And, a diagnostic implementation is resource intensive as all analysis has to be made on the device's upper SW layers. For many LRUs this imposes unrealistic overhead due to its need for CPU/MCU data processing tasks and associated cost increases. For this reason the US government institutions funded and continues to fund research projects to investigate the potential benefits for defining the features of a built-in connection status monitor. It is obvious that such research is only possibly when prototyping, testing and evaluating the solution in a flexible platform, i.e. an IP core running on a suitable FPGA.

b) Optimization of IEEE1394 devices for the use in AS5643. As mentioned before IEEE1394 was designed for the utilization in an open network. It allows devices supporting different "levels" to interconnect and communicate on the same bus. An example is the device speed, meaning that nodes supporting different speeds of S100 up to S3200 can be interconnected. As part of the bus reset phase they would negotiate the adequate interconnecting speed via a process called toning. While this process is useful in the consumer electronics world it is very much undesired in A&D. Pretty much all avionics programs define a network speed and all connected devices have to operate on that speed. Therefore, the toning process described above is not needed and the extra time spent on its execution is very much unwanted in a time critical control bus like the avionics data bus. "Setting" the operations of a device to a certain speed requires various versions of COTS silicon in the traditional silicon approach due to the variations on network speeds used throughout the industry. Fortunately, such settings can be easily realized in IP and FPGAs. An implementation in the SW layers is not possible in this case.

c) Several A&D programs have shown interest in using standard IEEE1394 isochronous streaming together with typical AS5643 ASM streaming. While fundamentally allowed, the different time synchronization references - Cycle Start (CS) in IEEE1394 and Start of Frame (STOF) in AS5643 – make the process tricky for maintaining the precise timing in both time domains. Yet, customizing the IEEE1394 transmission mechanism to allow for isochronous streaming without Cycle Starts – or alternatively synced to the STOFs - would be interesting options to explore.

d) Implementation of AS5643 using COTS silicon has been plagued with shortcomings, incompatibilities and bugs. For example, errors in the PHY state machine cause Bus Reset storms that severely impact the response cycle in a time-critical avionics control system. And the spec's default values in acceptable errors in faulty transmission causes port disconnects and therefore instable topologies. Such critical behavior can be enhanced, optimized as well as customized to meet specific requirements, environments and connectivity challenges. The complexity and dynamics of these problems can often only be addressed on a case-by-case basis and make a fix within standard silicon rather difficult, limited and restrictive.

Many more examples for the benefits of such an IP approach can be found and described. And they all enhance the functionality, stability, reliability and maturity of AS5643. Yet, listing them all would deviate from the main intention of this white paper.

4 FPGAs in A&D

For several years risk mitigation concerns (for example the maturity level of reconfigurable FPGAs and consequences of their usage) had effected the adoption of field programmable gate arrays within A&D programs. And that had not entirely been the devices' fault. Very likely the entire industry had not been ready for "changeable

HW". Traditionally, hardware (electronic components and subcomponents) had been seen as "static devices" with established processes on replacement, modifications, upgrading, etc. "Flexible approaches as provided by FPGAs require adaptation of these processes as reconfigurable HW (i.e. Firmware) needs to be handled more like SW. Lately, the A&D industry seems to be getting a better handle on this issue and appears more open to FPGA enabled solutions.

Additionally, FPGAs have become more resistant to the impact of radiation effects. Radiation hardening is a serious concern not only to space applications but also for civil and military applications due to the HW's high altitude exposure and mission length. Yet, in recent years we have seen significant advances in radiation hardening. Various technologies implemented by FPGA device manufacturers have reduced the consequences of radiation while offering much higher stability and reliability.

5 Conclusion

FPGAs are becoming widely accepted in avionics applications due to their significant advantages for introducing technological innovation. Furthermore, the need for customized solutions, critical bug fixes together with specific enhancements for the IEEE1394 and AS5643 interface is gaining in importance in order to provide more reliable, stable and mature avionics systems. Looking at it in the big picture, IP-based AS5643 interface solutions can be the trigger for a new generation of AS5643 functionality, interface definition and system performance. At a minimum IP solutions can be a development bread-boarding and testing platform for a later integration within silicon or ASICs. However, with modern FPGAs becoming more powerful together with affordable pricing, the costs for such silicon development, testing and verification likely will become prohibitive.