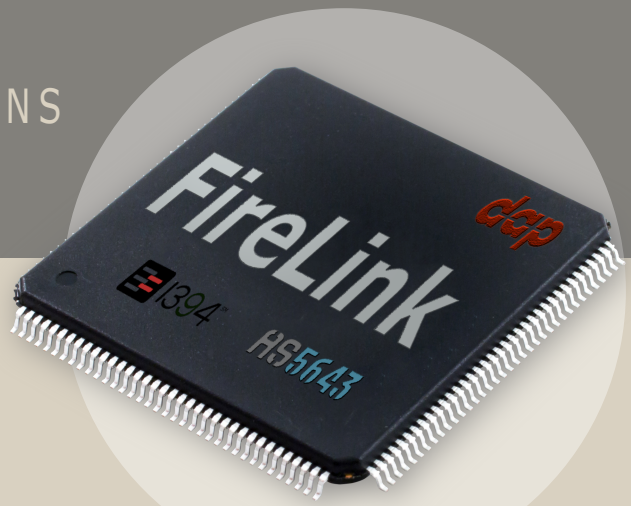
dap TECHNOLOGY

IP SOLUTIONS

FIRELINK

FLx-yyy



- yyy: NetList / SourceCode / Deployment
- x: Basic / Extended / GPLink
- FL: FireLink

1394SM

MIL1394

INTRODUCTION:

This datasheet describes the FireLink® IEEE1394b Link Layer Controller Cores from DapTechnology. The synthesizable IP core is based on the Link Layer Controller that has been used for several years in the FireWire analyzers produced by DapTechnology. And since its release the core has been successfully used within several 1394 applications. The code is written in VHDL and evaluation platforms are currently available for Xilinx and Altera FPGAs.

The FireLink® LLC provides the control for transmitting and receiving 1394 packets, including asynchronous packets, isochronous packets and PHY packets, at speeds up to 3200 Mbps (S3200). The LLC can be interfaced to either a PHY-chip, or to the DapTechnology FireGate PHY-IP which can be integrated in the same FPGA.

DapTechnology offers three versions of the Link Layer Controller to the market, i.e. a *Basic,* an *Extended* and the *General Purpose Link (GPLink)* version. The Basic version is optimized for small core sizes whereas the Extended version aims for high bandwidth throughput. And GPLink is a replacement for commercially available general purpose chips. All versions have their respective feature sets and benefits. DapTechnology will gladly assist customers in selecting the appropriate version for their particular product.

Key Features

- IEEE 1394b-2008 compliant
- Supports 100 - 3200 Mbps data transfer rates depending on target platform specifications
- Supports Legacy and Beta packets RX/TX (depending on the connected PHY)
- Software support via Dap's own 1394 SW stack FireStack®
- OHCI compliant (Extended version)
- Supports all standard 1394 packet types
- Configurable Cycle Master capability
- Maximum isochronous packet size 8KB (S800), 16KB (S1600) and 32KB (S3200) (for Basic version & depending on buffer size)
- Isochronous and Asynchronous packet filters
- Automatic Acknowledge generation depending on Link Layer Controller state, packet type and available buffer size
- Various forced errors, including:
  - Symbol
  - Header CRC error
  - Data CRC error
- PHY clock optional asynchronous to host clock
- Basic: Isochronous transmit/receive ports for up to 8 channels
- Compatible with Texas Instruments Physical Layer Controllers

AS5643

Several market segments can leverage the DapTechnology FireLink® IP Core due to the unique features of the solution. Good examples are Aerospace & Defense, Industrial, and Consumer Electronics industries. As a special option, the FireLink® LLC Extended offers Firmware Support for the SAE AS5643 protocol. While current implementations require significant host SW support, the FireLink® can support this layer with significantly better timing as well as reduced host resource utilization. Typical examples of applications in aerospace & defense for the FireLink® would include command & control systems for space-based vehicles, missile platforms, and fighter aircraft, as well as its implementation in avionics & IFE platforms for military, business and commercial aircraft.

COMMON FEATURES:

Host Bus Interface

The following types of host bus systems are supported:

- *Generic:* A generic 32-bit synchronous host bus.
- *PLB:* A 64-bit synchronous bus used in Xilinx FPGAs for their MicroBlaze and PowerPC based systems.
- *Avalon:* A 32-bit synchronous bus used in Altera FPGAs for their NIOS processor (Basic only).
- *AXI:* 32-bits wide bus used in MicroBlaze and ARM-based systems.
- *APB:* 32-bits wide bus used in Microsemi FPGAs

The Basic and GPLink versions are implemented as a slave-only bus interface, while the Extended version utilizes a DMA engine which accesses the bus as a Master.

Control Status

All versions have a number of registers that are used to control the Link Layer Controller and to check its status. For the Extended version, control for the DMA engine is also provided according to the OHCI standard.

CRC Calculation/Verification

Data and Header CRC are automatically added for Outgoing Packets. CRCs are verified for incoming packets. Faulty packets are ignored. Additionally errors can be injected for TX packets (symbol, header and or data CRC).

Ack Generation

Acknowledge Packet Generation is based on incoming packet content, available buffer space as well as LLC state.

Filtering

NodeID (async) and channel number (iso) specific packet filter engine.

ISO Ports (Basic version only, optional)

Up to eight (8) independent ISO Receive or ISO Transmit ports are provided. The purpose of these ports is to connect dedicated stream HW (e.g.: image/video generating/receiving HW) for the handling of data streams without burdening the host processor.

Received and Transmitted isochronous packets can be routed through the ISO Ports therefore providing a dedicated and highly efficient data path for the isochronous packets. Optionally the packet headers will be skipped (RX) or automatically generated (TX).

Async Receive Port (Basic version only, optional)

FireLink Basic has an option to route received asynchronous packets to an asynchronous receive port.

Cycle Start Generation (optional)

A Cycle Start Packet generation functionality with its associated Cycle_Time Register is supported by the HW. The feature can be enabled disabled as needed.

Other Options

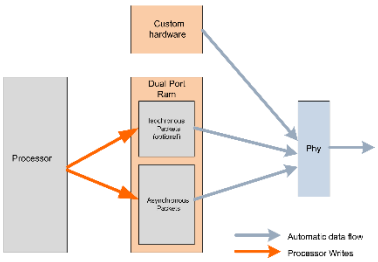
Please discuss other requirements with Dap Technology. We will provide you with a feasibility analysis as well as involved costs/lead times.

1) THE BASIC VERSION:

Processor-driven communication:

In the *Basic* version the packet data flow is processor driven, i.e. any received/transmitted packets have to be read from or written to a Dual-Ported RAM Buffer by a processor. The Dual Port RAM Buffer is located inside the core and is customizable in size to accommodate for the maximum packet size.

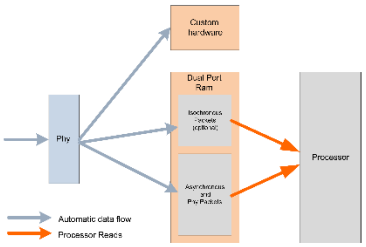
This concept is intended for small core sizes.



Packets to be transmitted are written into the Asynchronous Transmit Buffer.

Isochronous packets can also be transmitted from the Isochronous Transmit Port.

Received Packets are stored in the Isochronous or Asynchronous Receive Buffer or are routed to an Isochronous Receive Port or the Asynchronous Receive Port.



Architecture:

FireLink® Basic consists of a fully IEEE1394-2008 compliant Link Layer implementation. All LLC related functional blocks (top section in the right hand graphic) ensure functional standard compliance as well as interoperability with off-the-shelf physical layer devices (assuming PHY layer I/O compliance).

Essential to FireLink® Basic is its very simple host connectivity. Via simple 32 bit data/address bus R/W operations as well as control registers. Updates can be handled via a dual-ported RAM or direct register access. Since any communication with this DPRAM is host processor driven this interface is optimized for small/medium sized data (isochronous, asynchronous and PHY layer) packets as well as low bandwidth requirements. Just like sending large amounts of data via the I/O bus, an increased number of individual bus transactions negatively affect the overall interface performance. For transmission and reception of large isochronous streams (e.g. video and/or audio) alternate data paths are available by means of the ISO Transmit and Receive Ports. They allow connecting dedicated data generating/processing HW directly to the transmit/receive engines of FireLink®. As these dedicated ports are bypassing the host main processor they are not restricted by performance limitations of the main host interface and therefore guarantee optimized data rates.

An additional benefit is the ability to customize several functional elements of the core. Since not all 1394 implementations require a full featured 1394 interface (e.g. a pure IPv4 (IP over 1394) or AS5643 implementation using only asynchronous messaging can reduce FPGA footprint requirements by leaving out certain functional blocks like isochronous data ports, Cycle Timer and transmit, etc. in the deployed netlist. Likewise, an isochronous data transmitting video camera can omit a RX iso port as it is a dedicated data streaming device and the general purpose RX and TX buffer can be held small.

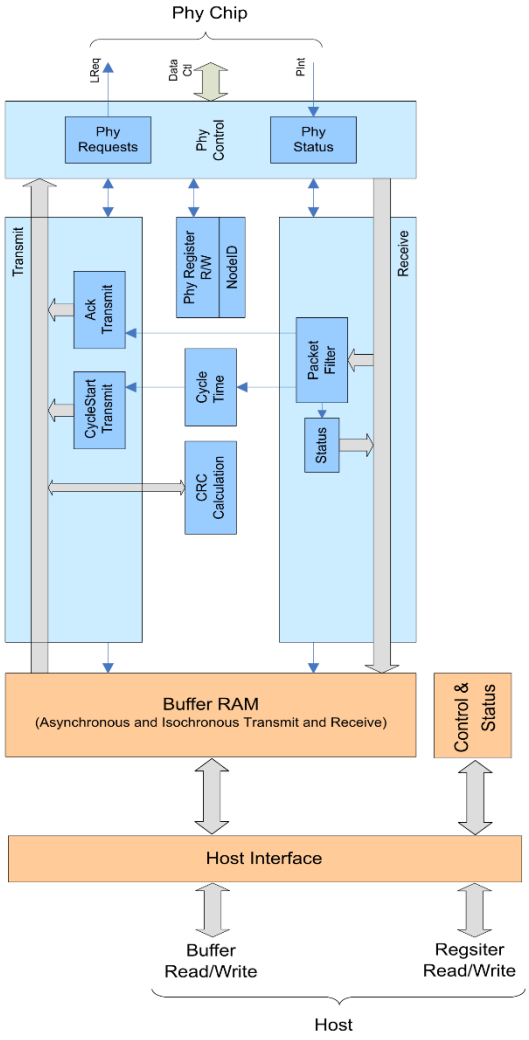
Typical Resource Utilization:

	Basic Version (Xilinx)
LUTs [2]	1400 – 2000
FFs [2]	700 - 1300
Block RAMs [2,3]	1 - 128
Host Bandwidth [1]	400 MByte/s (peak)
Buffer/FIFO size [2]	1K - 64K bytes
ISO Receive Ports	0 – 8
ISO Transmit Ports	0 – 8
Async Receive Port	0 – 1
# of DMA channels	-

[1] depends on host bus interface
[2] depends on FPGA type and selected options
[3] depends on needed FIFO size

Supported FPGA platforms

Xilinx	Spartan 6 Virtex-5, Virtex-6 Kintex-7
Altera	-
Microsemi	-

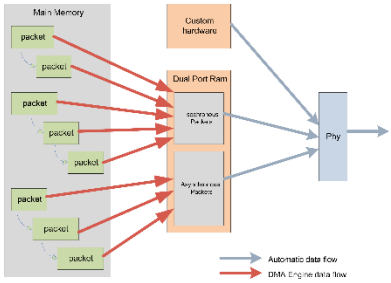


2) THE EXTENDED VERSION:

DMA-driven communication

In the *Extended* version the packet data flow is DMA driven. It is an OHCI compliant implementation with optional extensions using descriptors and packet buffers. The LLC's DMA Engine handles the transfer to/from a FIFO Buffer for receiving and sending packets automatically, enabling high bandwidth systems. The user creates lists of packets to be sent and/or cyclic buffers for packets to be received. The FIFO is located inside the core and its size is customizable to accommodate host bus latency.

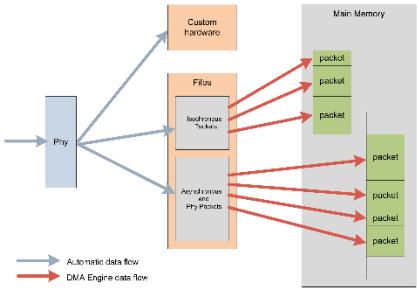
This concept is ideal for high-bandwidth applications. The concept reduces processor load.



Packets to be transmitted are read from a chain of packets stored in host memory. There may be a separate chain for asynchronous packets and each channel for isochronous packets.

Received packets are stored in chained buffers which are prepared in host memory.

A new buffer can be used for each packet, or multiple packets can be stored in one buffer. For certain applications, like camera streaming, the LLC is capable to stream the packet payload immediately into video buffers, with an absolute minimum of processor overhead



Architecture:

FireLink® Extended and Basic both contain the same LLC related functional blocks (top section in the right hand graphic) and with that ensure functional standard compliance as well as interoperability with off-the-shelf physical layer devices (assuming PHY layer I/O compliance).

The big difference between the two versions lies in the host connectivity interface. FireLink® Extended utilizes the architectural and performance-based benefits of the DMA capable communication interface. DMA transfers copy blocks of memory from one device to another and, while the CPU initiates the transfer by issuing a DMA command, it does not execute it. Advanced bus designs such as PCI typically use bus mastering DMA where the device takes control of the bus and performs the transfer itself. In an embedded processor or multiprocessor system-on-chip, it is a DMA engine connected to the on-chip bus that actually administers the transfer of the data. Another difference is that the Extended version does not include iso ports as the DMA mechanism efficiently handles the iso data transfer.

FireLink® Extended uses such an advanced DMA-enabled interface. And FireStack® - Dap's own IEEE1394 software stack – takes this concept even further with its consistent utilization of zero-copy data handling mechanisms. Together they form a very powerful combination aimed at complete system throughput optimization as well as minimization of system latencies and resource utilization.

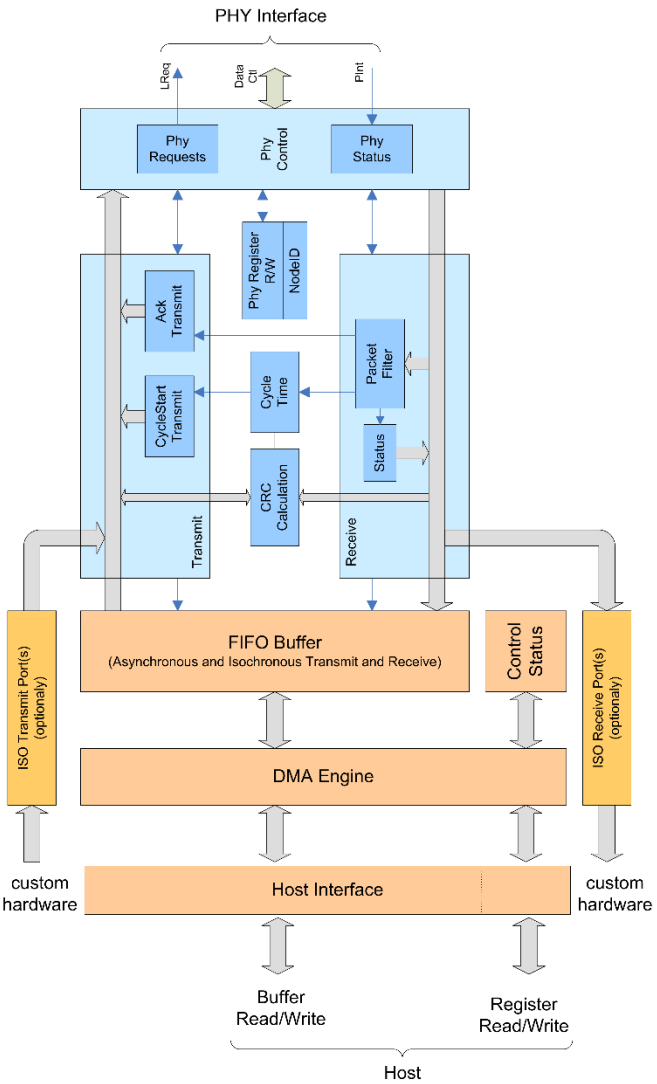
Typical Resource Utilization:

	Extended Version* (Xilinx)
LUTs [2]	2200 - 3000
FFs [2]	1500 - 1900
Block RAMs [2,3]	1 - 128
Host Bandwidth [1]	500 MByte/s (peak)
Buffer/FIFO size [2]	1K - 64K
# of DMA channels	4 - 68

[1] depends on host bus interface
[2] depends on FPGA type and selected options
[3] depends on needed FIFO size
* details to be finalized

Supported FPGA platforms

Xilinx	Spartan 6 Virtex-5, Virtex-6 Kintex-7
Altera	-
Microsemi	-



3) THE GPLink VERSION:

A chip replacement

The SAE AS5643 compliant FireLink GPLink IP Core is targeted at applications requiring a replacement for the currently used general purpose Link Layer Controller chips. FireLink GPLink has all functional blocks typically required for A&D implementations.

The DapTechnology implementation is focused on AS5643 applications which often require flight-ready hardware and consequently DO-254 certification. Therefore, the FireLink GPLink must be DO-254 certifiable IP which requires significant resources. Certain unused features (Iso TX/RX, Cycle Start, Cycle Master) of commercial silicon are not implemented in order to minimize the footprint.

Key Features

- IEEE-1394b-2008
- Supports S100 - S400 transfer rates
- IP-Link Layer
- 2 Kbytes asynchronous transmit FIFO (ATF)
- 2 Kbyte general receive FIFO (GRF)
- 16-bit handshake mode microcontroller interface
- Microcontroller rates up to 60 MHz

Architecture:

FireLink GPLink consists of a fully IEEE-1394b-2008 compliant Link Layer implementation. All LLC and PHY related function blocks ensure standard compliance as well as interoperability with off-the-shelf network devices (assuming PHY layer I/O compliance).

The microcontroller interface allows the microcontroller to communicate with the internal control and configuration registers (CFR), asynchronous transfer FIFO (ATF), and general receive FIFO (GRF), each of 520 quadlets (2 Kbytes) using a native interface. All microcontroller RX/TX operations are initiated by the microcontroller.

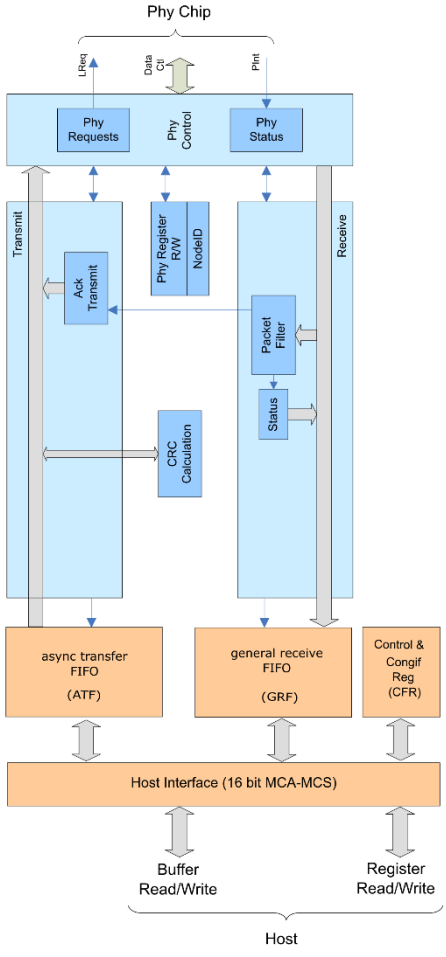
Typical Resource Utilization:

	GPLink Version (Microsemi)
LUTs [2]	
FFs [2]	
Block RAMs [2,3]	
Host Bandwidth [1]	
Buffer/FIFO size [2]	Details available under NDA
ISO Receive Ports	
ISO Transmit Ports	
Async Receive Port	
# of DMA channels	-

[1] depends on host bus interface
[2] depends on FPGA type and selected options
[3] depends on needed FIFO size

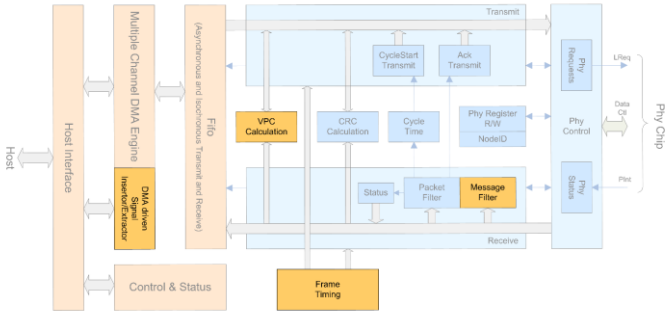
Supported FPGA platforms

Xilinx	Virtex-6Spartan-6 Virtex-5, Virtex-6, Virtex-7 Artix-7 Kintex-7
Altera	-
Microsemi	-



AS5643 EXTENSION:

DapTechnology offers a very unique, but extremely powerful addition to its standard 1394b link layer IP core (Extended version only). Our active participation in SAE ASD AS-1A3 standards committee together with the close collaboration with many adopters of the this standard allows DapTechnology to, not only develop a fully standards-compliant extension to the LLC, but also go beyond and/or deviate from the current AS5643 standard.



AS5643 additions to extended version of FireLink LLC

The AS5643 package is designed to offload the AS5643 support for the host processor. The following features are supported in firmware:

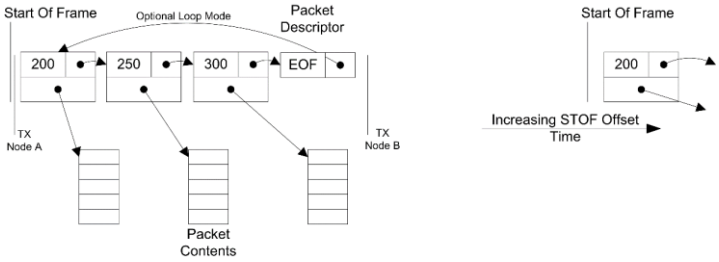
- AS5643 Protocol timing
  - STOF Generation: Accuracy: 0.3 µsec
  - TX Frame Offset Time: 0.3 µsec
  - RX Frame Offset Time Stamps: Accuracy : 0.3 µsec
- AS5643 Protocol encapsulation
  - Vertical Parity Check Insertion and Verification
- Hardware RX Filter on ASM MessageID and/or Channel

Compared with other implementations using off-the-shelf 1394 LLC silicon (and AS5643 support implemented in SW) this AS5643 extension to the extended version of FireLink drastically improves the overall system performance, offloads the host processor and guarantees timing deadlines that otherwise can only be accomplished with real-time operating systems.

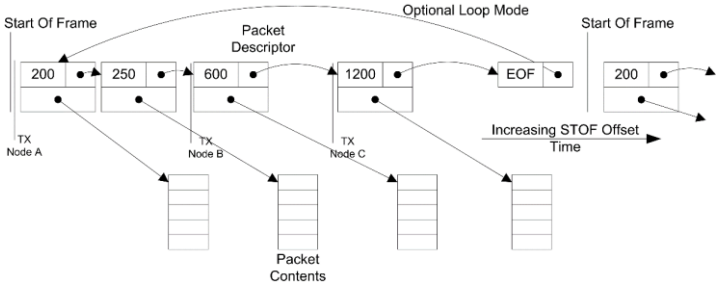
FireLink can also be paired with FireGate. With their respective AS5643 extensions they form the perfect PHY/LLC system on the chip (SOC) solution for typical aerospace applications. Please contact DapTechnology if your requirements go beyond the current AS5643 specification. The flexible architecture of the AS5643 extensions allows for the integration and support of features/functions that were not considered in the AS5643 standard as they are not supported by standard silicon.

AS5643 MESSAGING:

The AS5643 solution takes full advantage of the OHCI-like system architecture of the extended version of the FireLink®. From an applications point of view the OHCI-like descriptor block model is perfectly suited for powerful transmission linked lists for asynchronous stream packets. Part of the descriptor is a 16-bit timing field which allows for a precise frame time offset as required by AS5643. Additionally, the descriptor can be run in a looped mode in case a device has to transmit in every STOF frame.

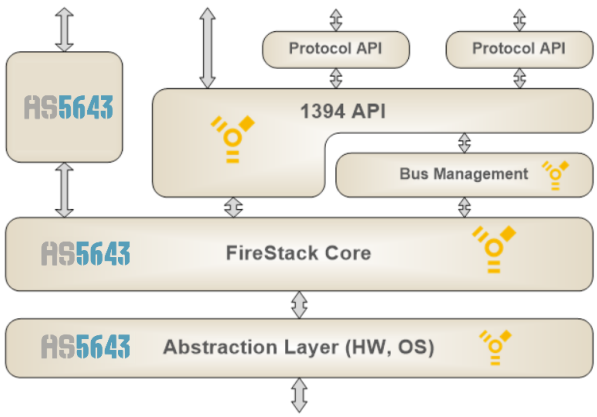


The same mechanism also allows transmitting messages from a single device but utilizing different node specific time slots. Such transmission lists can be perfectly used for simulation projects that may want to simulate an entire network's traffic without physically using multiple bus devices.



SOFTWARE SUPPORT:

In order to support FireLink DapTechnology has developed its own SW solution FireStack®. This innovative SW stack was architected from ground up in order to support the advanced features of the FireLink® IP Extended solution. It complies with IEEE1394 requirements as well as select higher protocol layers e.g. IIDC). And as the only product in the market it natively supports AS5643 features and functions.



PRODUCT POSITIONING:

This FireLink® IP Core is targeted at applications with up to 3200 Mbps data transmission requirements and for designs with or without a PCI Link Controller requirement. Any existing designs based on the (TSB12LV32) will greatly benefit as the FireLink® architecture shows many similarities. And with the Extended version, products requiring DMA capabilities can easily be paired with off-the-shelf PCI IP cores or bridge chips.

The industrial applications of FireLink® are quite broad and include robotics, machine vision, wide format digital printing and medical imaging. Finally, the FireLink® LLC Core is ideal for use in Consumer Electronics equipment such as Set Top Boxes, DVD peripherals and High Definition A/V equipment.

FireLink® was the first IP solution to transcend IEEE-1394 beyond S800. And with FireGate® and FireStack® it offers a complete package for a complete 1394 bus I/O solution that is able to address the growing demands for speeds beyond S800.

Evaluation Platforms:

Several evaluation platforms are available, for example:

- Xilinx ML507 (Virtex)
- Xilinx KC705 (Kintex)
- Xilinx AC701 (Artix)
- Microsemi M2S150TS (SmartFusion2)

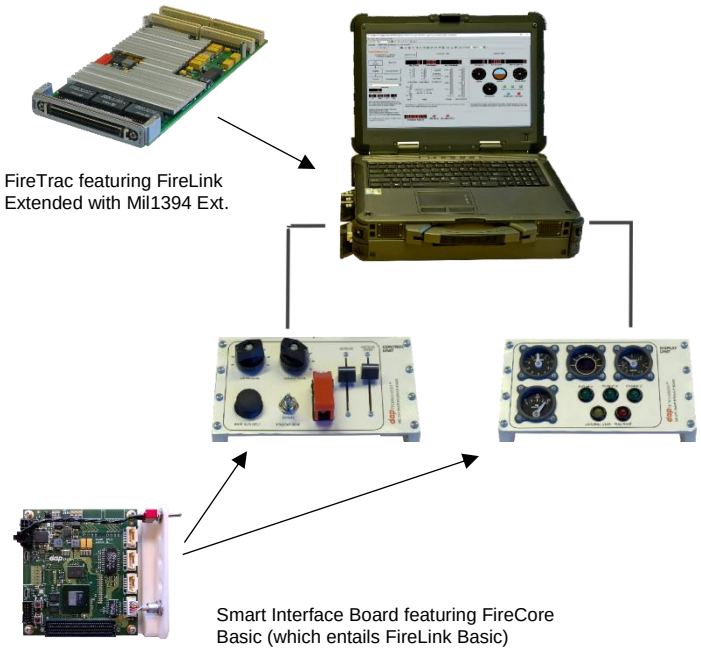
The 1394b physical layer extension is accomplished via a 1394b PHY adapter board EZPHY800. A TSB81BA3 PHY from Texas Instruments is mounted on the add-on board that is delivered with the package.

Please contact DapTechnology for more information on the various evaluation platforms as well as their availability.

AS5643 COCKPIT DEMO

DapTechnology's FireLink® IP core is an integral part of AS5643 Cockpit Demo showcase. This reference platforms simulates an AS5643 network on several levels and utilizes the FireLink IP core in several ways:

a) FireLink Extended is used as a IP Link layer in FireTrac which itself is part of the laptop system (together with a FireSpy). In this setup the core uses the extended OHCI functionality as well as the AS5643 features to take full advantage of the FireLink Extended benefits for simulating a vehicle management control (VMC) system.



FireTrac featuring FireLink Extended with Mil1394 Ext.

Smart Interface Board featuring FireCore Basic (which entails FireLink Basic)

b) DapTechnology's Smart Interface Board provides the network interface as well as engine to drive the Control Unit as well as the Display Unit. Both platforms are running Remote Node software on a soft-core MicroBlaze processor which is connected to a FireCore Basic IP core. FireCore Basic includes both FireGate and FireLink Basic IP cores. The current iteration of this Demo runs on Xilinx FPGAs but DapTechnology plans to upgrade the Smart Interface Board platform to Microsemi shortly.

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