dap TECHNOLOGY

IP SOLUTIONS

FIREGATE

FG-yyy

NetList / SourceCode / Deployment

FireGate

1394SM

MIL1394

PRODUCT OVERVIEW:

With its IEEE-1394 IP core product line DapTechnology has set an example for industry leadership and a keen technology vision. **FireGate** complements this successful series with a full featured PHY IP core. Not only does DapTechnology add its industry-proven Link-layer IP solution **FireLink®** but also the complex PHY layer boasting transmission speeds up to S3200 to its product portfolio. And when paired, FireLink & FireGate can be combined into one single FPGA as **FireCore**, i.e. a fully integrated field programmable system-on-the-chip (SOC) solution that clearly aims to take the integration of 1394b to the next level.

Transmission speeds beyond 800 Mb/s for FireWire have become a real requirement. The need originates mainly from bandwidth rich applications in the video and audio arena. Even with the current industry standard of 800 Mb/s, there are restrictions in the amount of video data that can be transmitted, especially when dealing with high-resolution, uncompressed video streams. While quite common and generally accepted in the consumer video arena (MPEG or DV video compression) in practically all industrial, medical, scientific and avionics applications, lossy compression algorithms are not usable and the size of video data streams is constantly increasing. Likewise, the number of simultaneously transmitted streams is rising as well for typical applications.

Over the years DapTechnology has established itself as an industry leader for FireWire related IP solutions. The company has gained experience with the specifics of FireWire PHY technology during the development of the InvisiPHY® technology which resulted in the unique FireStealth® analyzer and related IP solutions. Leveraging on this experience Dap launched the development of a Beta-only FireWire PHY solution called **FireGate** and successfully established means to utilize the transceivers inside modern FPGAs. Such an approach has resulted not only in high speed abilities (800Mb/s (S800), 1600Mb/s (S1600) or 3200Mb/s (S3200)) but also in quite interesting expansion capabilities as required for aerospace and industrial applications with their unique project specific needs for slower speed (100Mb/s (S100), 200 Mb/s (S200) and 400Mb/s (S400)).

Key Features

- IEEE 1394b-2008
- Supports S100b, S200b, S400b, S800b, S1600b and S3200b (supported speeds depend on the particular FPGA device)
- Complete IP solution that can be paired with standard LLC silicon or FireLink®
- Flexible number of PHY ports
- Future support for SAE AS5643 and further enhancements
- Supported by Xilinx Virtex-5, Spartan6 (S1600), Virtex-6 and Kintex-7 FPGAs
- Supports Microsemi SmartFusion2 and IGLOO2 (selected speeds)

SPECIFICATION:

Please contact DapTechnology for detailed product specifications.

DESIGN FEATURES AND BENEFITS:

There are several advantages when using FPGAs to implement a PHY. Some of these are:

Single-chip solution: The PHY IP can be combined with Link Layer IPs, creating smaller, compact solutions. Additional components can be added to create a System-On-Chip (SOC) solution.

Flexible number of ports: Commercially available PHY chips have a fixed number of ports. Small peripherals can benefit from having only one or two ports. Host adapters would likely benefit from 3 or more ports and a hub could even have more than that. For a PHY based on FPGA technology, the user can customize the number of ports as required.

Optional debug and test features: Optionally the user can include debug and test features such as BERT (Bit Error Rate Test) Low level data monitoring and recording.

Field-upgradable: The used FPGAs are field upgradable thus allowing the addition of new features or fixing of bugs, even with the device already deployed in the field.

Cost effective ASICS: Once a design is finalized an IP solution offers a very cost effective path to rendering a custom ASIC.

ADDED AS5643 FEATURES:

FireGate also offers unique possibilities to optimize standard 1394 features for their use in typical A&D applications. Since off-the-shelf silicon solutions are not specifically addressing this industry's unique requirements, "work-around" specifications (SAE AS5643) have been developed. FireGate on the other hand offers the possibility to address critical issues from the onset and will allow for the development of solutions perfectly suited for mission critical and even space-borne applications. Especially in combination with the AS5643 enhancements offered by FireLink® highly optimized solutions can be created.

Please contact DapTechnology directly for the AS5643-SOC Whitepaper (NDA required).

AS5643

LICENSING OPTIONS:

Three different IP license types are available for this product:

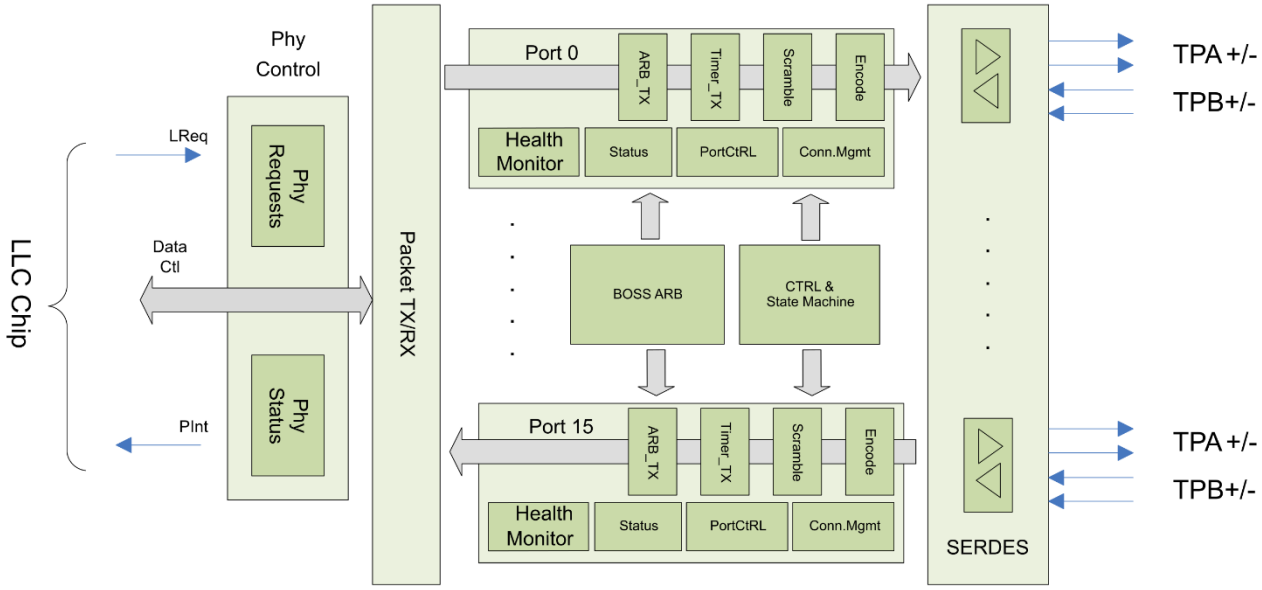
NetList: customers receive complied VHDL code that can be synthesized to render a gate level hardware mapped representation of the design

SoureCode: license includes the right to use the VHDL source code

Deployment: Right to instantiate the IP on deployed products. Applicable to both Netlist as well as SourceCode licenses.

Architecture:

FireGate is a highly optimizes PHY solutions and works together with DapTechnology's FireLink implementation.



It presents a fully IEEE1394-2008 compliant PHY Layer implementation. The main PHY layer related functional blocks ensure functional standard compliance as well as interoperability with off-the-shelf physical layer devices. The PHY/Link layer interface has been optimized for performance and deviates from the standardized PHY/LLC interface. FireGate is optimized to work with FireLink which also supports these enhancements. It is not recommended to pair FireGate this off-the-shelf Link layer devices.

A key element of FireGate is its configurable PHY front end, i.e. the ability to customize several aspects of the PHY cable environment interface. During the configuration phase the total number of available PHY ports can be adjusted (max 16) and as well as the total number of PHY instances per FPGA device. Furthermore the speeds supported by the PHY can be defined. The PHY speeds can be either predefined to support single network speeds (for example S100, S200, S400, ...). This reduces network speed negotiation times (only applicable if the entire network would use the same PHY). Alternatively, the PHY(s) can be configured to support speed ranges (e.g. S200 - S800) and limit the speed negotiation to those values).

Additionally, the PHYs also contain patented connection diagnostic and health monitoring capabilities. Dap has been one of the very first companies to actively advocate such functionalities with PHY devices.

REFERENCE SYSTEM(S):

- A complete Xilinx S3200 reference system is available, including a 4-lane PCI-express host adapter, an S3200 FireWire analyzer and a peripherals development board which can be used by the customer to develop their products.

- Dap is currently working on a reference system for low speed (S100/S200/S400) Xilinx as well as Microsemi platforms.

CONTACT INFORMATION:

sales@daptechnology.com
www.daptechnology.com

DapTechnology B.V.
Beatrixstraat 4
7573AA Oldenzaal
The Netherlands
Ph: +31 541 532941

DapUSA, Inc.
780 W San Angelo Street
Gilbert, AZ 85233
United States of America
Ph: +1 480 422 1551

DT-PRO023DAT550E, MAR2021